REMARKS

This Amendment is filed in response to the Office Action dated December 14, 2004. For the following reasons this application should be allowed and the case passed to issue. No new matter is introduced by this amendment. The amendment to claim 10 is supported by claim 11. New claim 21 is supported by claims 10, 15, and 16. Support for new claims 22 and 27 is found in claim 20. New claim 23 is supported by claims 10 and 12 and the specification at page 6, line 28 to page 7, line 1, and FIG. 4 which discloses that the gate oxide layer is formed immediately adjacent to and in contact with the SiGe layer in the first region. Support for new claim 24 is found in claim 11. Claims 13 and 14 provide support for new claims 25 and 26, respectively.

Claims 10-27 are pending in this application. Claims 1-9 have been canceled. Claims 10-12 and 15-20 are rejected. Claims 13 and 14 are objected to. Claims 10 and 11 have been amended in this response. Claims 21-27 have been newly added.

Claim Rejections Under 35 USC § 103

Claims 10-12 and 15-20 were rejected under 35 USC § 103(a) as being unpatentable over Fitzgerald (U.S. Patent No. 6,724,008). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the instant invention as claimed and the cited prior art.

An aspect of the invention, per claim 10, is a method of manufacturing semiconductor devices comprising providing a semiconductor substrate comprising a SiGe layer formed on a base layer and a silicon layer formed on the SiGe layer. The semiconductor substrate comprises one or more first regions and one or more second regions spaced apart from each other by interposed isolation regions. At least a portion of the silicon layer is selectively removed only in the one or more first regions. A p-type dopant is implanted in the one or more first regions and

an n-type dopant is implanted in the one or more second regions. A gate oxide layer is formed in the one or more first regions and the one or more second regions. A gate electrode layer is formed over the gate oxide layer.

Another aspect of the invention, per claim 21, is a method of manufacturing semiconductor devices comprising providing a semiconductor substrate comprising a SiGe layer formed on a base layer and a silicon layer formed on the SiGe layer. The semiconductor substrate comprises one or more first regions and one or more second regions spaced apart from each other by interposed isolation regions. At least a portion of the silicon layer is selectively removed only in the one or more first regions. A dopant is implanted in the one or more first regions and the one or more second regions. A gate oxide layer is formed in the one or more first regions and the one or more second regions by oxidizing the silicon layer to form the gate oxide layer. Substantially all of the remaining silicon layer in the one or more first regions is oxidized to form the gate oxide layer.

Another aspect of the invention, per claim 23, is a method of manufacturing semiconductor devices comprising providing a semiconductor substrate comprising a SiGe layer formed on a base layer and a silicon layer formed on the SiGe layer. The semiconductor substrate comprises one or more first regions and one or more second regions spaced apart from each other by interposed isolation regions. Substantially all of the silicon layer is selectively removed only in the one or more first regions. A dopant is implanted in the one or more first regions and the one or more second regions. A gate oxide layer is formed in the one or more first regions and the one or more second regions. The gate oxide layer is formed immediately adjacent to and in contact with the SiGe layer in the one or more first regions.

The Examiner asserted that Fitzgerald discloses the claimed method, including a SiGe layer 1304 formed on a base layer (1306, 1308) and a silicon layer that is selectively removed 1314 overlying the SiGe layer. The Examiner further asserted that Fitzgerald teaches that the SiGe layer is graded (FIG. 1).

Contrary to the Examiner's assertions, Fitzgerald does not suggest that a p-type dopant is implanted in the one or more first regions and an n-type dopant is implanted in the one or more second regions, as required by claim 10. As disclosed in the instant specification, the present invention combines the enhanced electron mobility through NMOS transistors comprising strained silicon channels with the enhanced mobility of holes through PMOS transistors comprising SiGe channels. The mobility of holes in a SiGe lattice is greater than the mobility of holes in either strained silicon or conventional silicon crystalline lattices and the mobility of electrons is greater in strained silicon than conventional crystalline silicon. Therefore, forming PMOS transistors with SiGe channels and NMOS transistors with strained silicon channels provides a more balanced CMOS device that operates at higher overall speed than a device in which the PMOS and NMOS channels comprise conventional silicon crystal lattices (page 3, last paragraph and page 4, 2d paragraph). Thus, implanting a p-type dopant in the one or more first regions and implanting an n-type dopant in the one or more second regions provides a more balanced CMOS device that operates at higher overall speed. Fitzgerald does not suggest that a p-type dopant is implanted in the one or more first regions and an n-type dopant is implanted in the one or more second regions. Fitzgerald also does not suggest the balanced, higher speed CMOS devices that result from the claimed process.

Fitzgerald further does not suggest forming a gate oxide layer in the one or more first regions and the one or more second regions by oxidizing the silicon layer to form the gate oxide,

wherein **substantially all of the remaining silicon layer in the one or more first regions is oxidized** to form the gate oxide layer, as required by new claim 21.

In addition, Fitzgerald does not suggest removing substantially all of the silicon layer in the one or more first areas and **forming a gate oxide layer immediately adjacent to and in contact with the SiGe layer** in the one or more first regions, as required by claim 23.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). There is no suggestion in Fitzgerald to a) implant a p-type dopant in the one or more first regions and an n-type dopant in the one or more second regions, b) oxidize the silicon layer to form the gate oxide layer, wherein substantially all of the remaining silicon layer in the one or more first regions is oxidized to form the gate oxide layer, and c) remove substantially all of the silicon layer in the one or more first areas and form a gate oxide layer immediately adjacent to and in contact with the SiGe layer in the one or more first regions, as required by independent claims 10, 21, and 23, respectively.

The mere fact that references can be modified does not render the resulting combination obvious unless the prior art also suggests the desirability of the modification. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Fitzgerald does not suggest the desirability of a) implanting a p-type dopant in the one or more first regions and an n-type dopant in the one or more second regions, b) oxidizing the silicon layer to form the gate oxide layer, wherein

substantially all of the remaining silicon layer in the one or more first regions is oxidized to form the gate oxide layer, and c) removing substantially all of the silicon layer in the one or more first areas and forming a gate oxide layer immediately adjacent to and in contact with the SiGe layer in the one or more first regions, as required by independent claims 10, 21, and 23, respectively.

The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.*, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1449 (Fed. Cir. 1997). There is no motivation in Fitzgerald to a) implant a p-type dopant in the one or more first regions and an n-type dopant in the one or more second regions, b) oxidize the silicon layer to form the gate oxide layer, wherein substantially all of the remaining silicon layer in the one or more first regions is oxidized to form the gate oxide layer, and c) remove substantially all of the silicon layer in the one or more first areas and form a gate oxide layer immediately adjacent to and in contact with the SiGe layer in the one or more first regions, as required by independent claims 10, 21, and 23, respectively.

In rejecting a claim under 35 U.S.C. § 103, the Examiner is required to discharge the initial burden by, *inter alia*, making **"clear and particular"** factual findings as to a **specific understanding** or **specific technological principal** which would have **realistically** impelled one having ordinary skill in the art to modify an applied reference to arrive at the claimed invention -

- not generalizations. *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 57 USPQ2d 1161 (Fed. Cir. 2000); *Ecolochem Inc. v. Southern California Edison, Co.*, 227 F.3d 1361, 56 USPQ2d 1065 (Fed. Cir. 2000); *In re Kotzab*, *supra*; *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). That burden has not been discharged, as the Examiner has provided no factual basis for modifying Fitzgerald's methods to obtain the claimed methods. The Examiner did not make the requisite "clear and particular" factual findings to support the conclusion that one having ordinary skill in the art would have been realistically led to the claimed methods of manufacturing semiconductor devices.

The only teaching of the claimed methods is found in Applicant's disclosure. However, the teaching or suggestion to make a claimed modification and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. The Examiner's conclusion of obviousness is not supported by any factual evidence. The Examiner has not provided a factual basis for asserting that Fitzgerald suggests the claimed methods. The Examiner's retrospective assessment of the claimed invention and use of unsupported conclusory statements are not legally sufficient to generate a case of *prima facie* obviousness. The motivation for modifying the prior art must come from the prior art and must be based on facts. The Examiner is not free to ignore the judicial requirement for facts. To do so is legal error. *In re Lee*, 277 F.3d 1338 (Fed. Cir. 2002). Applicant submits that the Examiner has not presented a prima facie case of obviousness for the instant claims.

The dependent claims are allowable for at least the same reasons as their respective independent claims and further distinguish the claimed invention.

Allowable Subject Matter

Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Applicant gratefully acknowledges the indication of allowable subject matter. Applicant does not believe it is necessary to rewrite claims 13 and 14 in independent form, as it is believed that independent claim 10 is allowable for the reasons explained *supra*.

In light of the above Amendments and Remarks, this application should be allowed and the case passed to issue. If there are any questions regarding these remarks or the application in general, a telephone call to the undersigned would be appreciated to expedite prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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